Electronics design breakthrough will reduce R&D time for new weapons systems

by William Engdahl

According to government estimates it now takes on the average about 15 years to design, test, develop, and deploy a new weapons system. This situation partly reflects the increasing sophistication of new systems as well as the absurd regulatory thicket of restrictions in defense subcontracting which has proliferated since the onset of Robert McNamara's "cost-effectiveness" at the Pentagon in the early 1960s.

One of the major obstacles to rapid development and deployment of new generations of offensive as well as defensive weapons systems is the time it takes to design a new electronic micro-sized circuit essential to any modern system. A number of companies and universities have been involved in attempts to apply the potentials of computer-aided design to solving this serious bottleneck. DARPA, the Pentagon's research arm, has funded university research for that purpose at the University of Utah and Berkeley, among others, and Boeing is said to have invested almost $3 million before shelving its attempt as unwieldy and impractical.

Following three years of intensive design and testing, a small company named Cademic in the growing new "Silicon Valley" near Phoenix, Arizona has created a major breakthrough in the design and manufacture of the extremely complex, extremely tiny micro-electronic circuitry integral to any new weapons system. One industry representative familiar with the new system insists that it will create a "potential revolution in the design phase" of microelectronic integrated circuits.

The new development in integrated circuit (IC) design and manufacture presents the potential to drastically change the organization of the electronics industry within a few years, if not months. The strategic implications of any such technological advance indicate the potential for rapid development of the U.S. economy under conditions of national mobilization of resources and talent.

Its developers state that the new approach, incorporated under the acronym of Cademic—Computer Aided Design, Engineering, Manufacture of Integrated Circuits—will make substantial cost and time reductions in design of new custom or application-specific integrated circuits, as they are called in the industry.

Today, a major aerospace-defense company such as Lockheed or Boeing may require 30 to 40 new circuit designs a year. It is not uncommon for a major company to spend from $500,000 to $5 million and 15 to 24 months on a major new circuit design and production project. By contrast, Cademic is able to accomplish the same for about $40,000 in a time-frame of 4 to 12 weeks. Cademic's developers say that with experience, it can reduce this to less than a week.

As an industry average, it takes approximately 18-24 months for the completion of design through successful manufacture and testing of a new micro integrated circuit chip. The problems attendant in these micro-miniature pieces of complex circuitry can mean the difference between deployment, for example, of a successful system of energy-beam defense against oncoming enemy missile attack, or not. In the realm of nuclear war, faulty design or manufacture has little place.

Manpower logjam

Currently, development of new integrated circuit designs is a highly skilled, largely labor-intensive process of producing from engineering specifications provided by electrical engineers multi-layered (often up to 14 layers) drawings which must then be manually "fitted" into given space requirements, optimally routed, and optimally interconnected between these layers. This part of the process of designing a new piece of integrated circuitry, the circuit design phase, is now a major bottleneck. Why?

According to a recent industry survey by LSI Logic Corporation, there are only 2,000 qualified IC circuit designers in the United States, of which only some 1,300 are active. These designers carry the burden of every new circuit needed, from sophisticated industrial robotics to new video games to circuitry for a new weapons system or satellites. Because of the enormous demand for these technicians, circuit-layout designers often command salaries in six digits and are generally overextended.

By comparison, there are some 220,000 electrical engineers currently working in the area of systems design, about half of whom, roughly 100,000, now work in the United States.

The major advance created by the Cademic system is that,

after a training seminar of a few days, any of these 220,000 electrical engineers who is capable of designing the external electrical circuit requirements for an integrated circuit or chip can design and execute the entire process of a new custom integrated circuit, all the way to chip manufacture, without need of any IC designer. This alone would solve a chronic obstacle to design and development of new circuitry for applications, especially in the technology-intensive area of defense electronics.

Computer-aided design

Computer-aided design and manufacture is of course a very active area of research activity in the electronics industry today. Known by the trade acronym CAD/CAM, these systems are now being used for a broad range of design problems, from garment manufacture to automobiles to industrial robots. Cademic's system, according to a number of industry people interviewed by *EIR,* is the only one known to work at present which breaks the manpower bottleneck at the engineer level rather than the layout-design level.

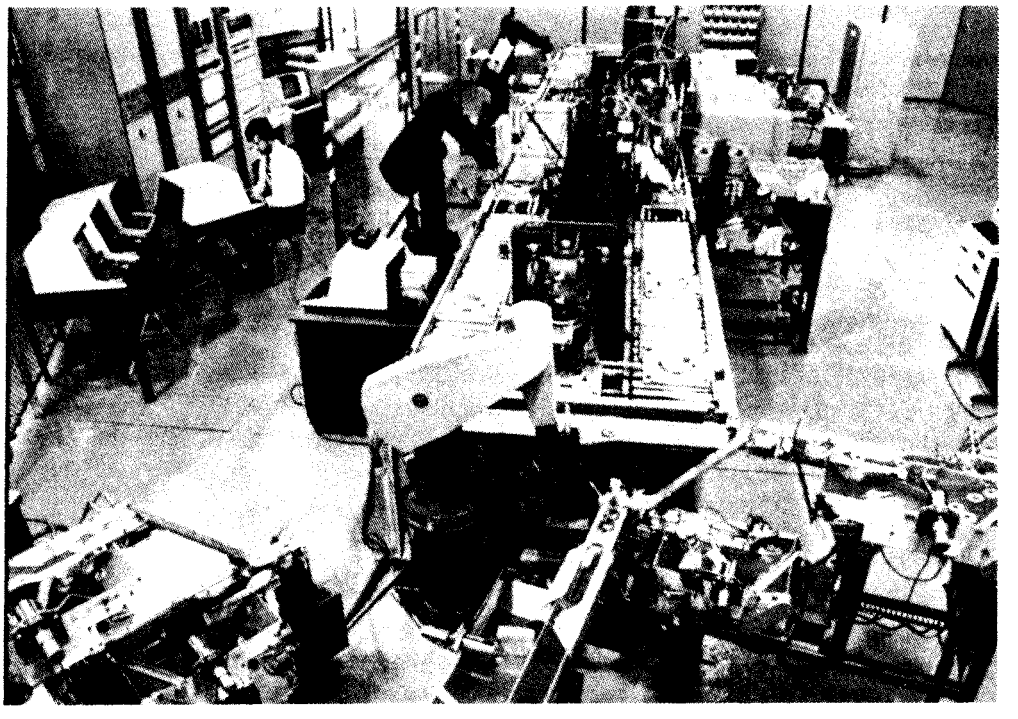
Some computer-aided design systems, such as the Mead-Conway system developed by Xerox and Berkeley, have much improved the productivity of the IC designer. But the absolute limit of only approximately 1,300 IC designers remains. Even if every one were diverted from current full-time commercial projects into development of the approximately 50,000-100,000 potential new designs estimated to be needed annually, barely a dent could be made.

As of this writing, though others can be expected to follow soon, Cademic uniquely allows the process of design of new integrated circuit systems to be accomplished in a fraction of the time and for a fraction of the normal cost. It can cut the average design time for production of a new integrated circuit from the current 18-24 months to approximately four to six weeks, about a 75% reduction, including several reworkings and de-bugging runs. Cademic can also effect cost reductions for production of new integrated circuits of up to 90%.

This means that testing and experimentation with new designs for such applications as guidance systems and missile circuitry would no longer be held hostage to various accounting methods which kill creativity and induce dangerous compromises in systems which can mean life or death.

Roger Bane, the founder of Cademic, which is based in Scottsdale, Arizona, took his 20 years' experience in the industry, gathered a handful of talented collaborators, and after three years of work, has perfected the first full "silicon compiler" in the industry, several years ahead of previous industry projections. The Compiler is a proprietary program which allows complete automation of the design of integrated circuits at the level of the electrical engineer, eliminating the bottleneck of circuit layout designer altogether.

Cademic's in-house Compiler is based on an extremely powerful VAX computer from Digital Equipment Corporation. In turn, Cademic licenses to its clients a "turnkey" package including a Design Editor and Logic/Timing Simulator together with licensed software. These tools enable the local electrical engineer to sit down at an engineering work station, a specialized computer terminal, work from his level of a circuit-logic diagram of the desired new design, and test the logic and the timing efficiencies of the design—a vital factor in complex microcircuitry. The Cademic-based Compiler translates this logic design from the engineer into an optimized geometrical configuration.



Advances in integrated circuit production are essential to the kind of adaptable programmable assembly system shown above.
Westinghouse Electric Corp.

"The Compiler starts from the standpoint of desired output [e.g. a circuit which will perform according to certain specifications in a given size configuration—W.E.]. We worked backward from the target of timing specifications," Bane emphasized to me in a recent interview. "Once we decided to do it, it was relatively simple. Timing is an input. Design is an input. Topological optimization is relatively easy. You 'squeeze the air out of it,' in a sense. The Compiler, which we spent three years perfecting, carries out optimization of the initial design. It isn't a simple one-to-one optimization. And it can't be reverse-engineered [replicating the design by obtaining a physical unit]."

Currently in the industry, using standard IC layout designers, routing optimization in the tiny and highly complex integrated circuit chips is a staggering problem. The packaging of highly complex circuits into systems of dimensions measured in microns is a major technological problem. Testing finished circuits is even more burdensome in time and cost.

The Cademic Compiler achieves power and ground optimization and optimization of signal path. Each work station is uniquely encoded for customer design security. Bane has created the only working silicon compiler which goes directly from a logic diagram to a custom integrated circuit untouched by human hands. Cademic's breakthrough could transform the entire micro-electronics industry, most importantly the defense and communications areas.

What the Compiler does more effectively than even computer-aided circuit layout designers is to optimize routing of the sometimes 14-level chip layers in a new wafer design. And far more than 1,300 people can potentially do such new design work with the use of the Cademic system. This may be Bane's most important contribution.

Cademic's Compiler design enables significant economies of production to be achieved in integrated circuit design as well. The Compiler produces a Pattern Generation (PG) tape from the initial logic input. This PG tape generates a "mask" analogous to a photographic negative. The mask is then used by a chip "foundry" to make the actual chip. Because of the nature of the Compiler's simultaneous optimizing capabilities, much smaller packaging can be achieved than by normal hand routing methods. Further, because of encoding procedures, Cademic can achieve substantial efficiencies in the foundry or production end; Cademic can test a number of different parts on one "wafer" even from different customers, because of uniqueness of encrypted coding. Thus they can provide a customer with manufactured chips far more cheaply because the system is able to "batch" many different designs onto one wafer.

The Cademic system has designed working chips already being used by at least one major instrument manufacturer. Delivery to customers of a newly upgraded design began at the end of 1983.

Quality control gains

A persistent problem in the development of sophisticated micro-electronics systems is testing for faulty chips. To "qualify" a typical 20,000-gate custom integrated circuit takes about eight years at present. As a result, the military uses custom parts only when absolutely necessary; this has been one of the major impediments to needed technological advance in weapons systems development. Currently the Department of Defense is carrying out an investigation of the U.S. semiconductor industry because of reports of deficient microchips and inadequate testing procedures. Obviously, detection of failure of a Poseidon missile under launch conditions is too late.

Present foundry production restrictions produce batches or runs of new chip wafers which yield an average of 20% "good" for 80% waste. Testing them is the most costly part of production of chips, and testing a new circuit design is enormously costly for this reason. Because of the Compiler design and built-in testing procedures, Cademic—as a by-product of solving another problem on the design bottleneck end—has now made possible important gains in the quality control area of integrated-circuit foundry production.

Cademic, by application of its Compiler on the levels of simultaneous optimization of design criteria cited above, eliminates problems from hand routing and enables foundry yields to soar from averages of 20% "good" to averages of 80%.

Further, because of how Cademic's Compiler must interface with a given foundry to input its pattern generation tape that's used to produce a mask and finally a finished wafer, their system has developed a master test which can also be used to "qualify" an entire foundry process line, not just individual parts for military specification purposes. Such a testing capability offers the military (as well as industry generally) a new tool to greatly aid in solving its staggering quality-control problems. At present there are 100-150 silicon foundries in the United States rated by class, e.g., Class 100, Class 10. This indicates the levels of air purity of parts per volume; purity is integral to chip reliability. There are only two or three in Class 10, none of superior rating. Japan is discussing design of a Class 1 foundry.

In the immediate future, application of the kind of breakthrough implicit in Bane's Cademic system may help solve major problems in design of custom high-speed integrated circuitry incorporating advanced "super-fast" materials such as gallium arsenide. Bane is certain his method will solve at least one big problem with using such sensitive new materials by permitting such circuits to be made "self-testing," which for considerations of space is now impossible in practice. This is the area of needed size-speed breakthrough which can permit early deployment of such systems as effective second-generation anti-missile energy-beam defense weapons requiring ultra-compact computers packaged in tiny satellites.